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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/691,353	10/18/2000	James W. Adkisson	BUR9-1999-0300-US1	3972

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EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/691,353	ADKISSON ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication app ars on th cover sheet with th correspond nce address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *2-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,14-19,22-28 and 30* is/are rejected.

7)☒ Claim(s) *20,21 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Response to Arguments

Applicant's arguments filed 03-20-2003 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 24-28 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Sano et al. (U.S. Patent 6,040,605).

Sano teaches a method of forming a field effect transistor (FET) transistor, comprising (See col. 9, line 50 to col. 10, line 14 and FIG. 1(b)):

forming a first semiconductor layer on the substrate 86 having first and second ends and a central region that is thinner than said first and second ends, said central region having first and second side surfaces;

epitaxially growing a semiconductor channel region 78 on at least one of said first and second side surfaces of said central region of said first semiconductor layer;

removing said central region of said first semiconductor layer;

forming a dielectric layer 81 on exposed surfaces of said semiconductor channel region; and

forming a gate electrode 80 on said dielectric layer;

The use of a combination of Group IV elements or an alloy of silicon and Group IV element in forming the semiconductor channel region is well-known to one of ordinary skill in the art of making semiconductor devices as recited in present claims 25-27.

The use of a material selected from the group consisting of polysilicon, silicon-germanium, refractory metals, Ir, Al, Ru, Pt, and titanium nitride in forming the gate electrode is well-known to one of ordinary skill in the art of making semiconductor devices as recited in present claim 30.

Claims 14-19 and 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Neudeck et al. (U.S. patent 5,273,921).

Neudeck teaches a method for forming a double gated field effect transistor (FET), comprising the steps of (See col. 5, line 4 to col. 8, line 35 and FIGS. 1A to 3J):

forming on a substrate 11 a first and second epitaxially grown channels;

Etching areas within a silicon layer to form a source 31 and a drain 32, wherein a side surfaces of the source 33 and the drain 34 contact opposing end surfaces of the first and second epitaxially grown channels; and

forming a gate (14, 20) that contacts a top surface and two side surfaces of the first and second epitaxially grown channels and a top surface of the substrate 11.

In re claim 15, Neudeck et al. disclose the method as recited in claim 14, wherein the forming step comprises the steps of:

forming first and second semiconductor line, each end of the silicon lines contacting one of the source 31 and the drain 32;

forming an etch stop layer 16 on an exposed side surface of each of the first and second semiconductor lines;

epitaxially growing first and second semiconductor layers on each etch stop layer 16;

etching away the first and second semiconductor lines and the etch stop layers 16;

filling areas surrounding the first and second epitaxially grown semiconductor layers and between the source 31 and the drain 32 with an oxide fill; and

etching a portion of the oxide fill to form an area that defines a gate,

wherein the area that defines the gate (14,20) is substantially centered between and substantially parallel to the source 31 and the drain 32;

In re claim 16, Neudeck et al. disclose the method as recited in claim 15, further comprising the steps of:

etching the oxide fill between the gate the source to expose the first and second epitaxially grown silicon layers;

and etching the oxide fill between the gate (14,20) and the drain 32 to expose the first and second epitaxially grown silicon layers.

In re claim 17, Neudeck et al. disclose the method as recited in claim 16, further comprising the step of forming an oxide on the first and second epitaxially grown silicon layers.

In re claim 18, Neudeck et al. disclose the method as recited in claim 17, wherein the oxide is silicon dioxide (20,21,22).

In re claim 19, Neudeck et al. disclose the method as recited in claim 14, further comprising the steps of:

implanting a portion of the epitaxially grown silicon layers between the gate 20 and the source 31;

and implanting a portion of the epitaxially grown silicon layers between the gate 20 and the drain 32.

In re claim 22, Neudeck et al. disclose the method as recited in claim 14, further comprising the step of forming a contact (33, 34) on each of the gate (14, 20), the source 31 and the drain 32.

In re claim 23, Neudeck et al. disclose the method as recited in claim 14, wherein the gate (14, 20) material is polysilicon.

Allowable Subject Matter

Claims 20-21 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Applicant's Arguments

Applicant's arguments filed 03-20-2003 have been fully considered but they are not persuasive.

In response to Applicant's argument that Sano fails to disclose removing the layer for exposing a second sidewall of the channel, Sano discloses removing the layer for exposing a second sidewall of the channel (FIGS. 1b and 16b and related text).

In response to Applicant's argument that Sano fails to disclose forming a first semiconductor layer having first and second ends and a central region that is thinner than the first and second ends wherein the central region having first and second side surfaces, Sano discloses forming a first semiconductor layer having first and second ends and a central region that is thinner than the first and second ends wherein the central region having first and second side surfaces (FIG. 1b and related text).

In response to Applicant's argument that Neudeck fails to disclose etching areas within a silicon layer to form a source and a drain, Neudeck discloses etching areas within a silicon layer to form a source and a drain (FIGS. 1-3 and related text).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
June 16, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800